

46

ABSTRACT OF THE DISCLOSURE

NSA 17

The present invention provides a system and method for improving the performance of general purpose processors by expanding at least one source operand to a width greater than the width of either the general purpose register or the data path width. In addition, the present invention provides several classes of instructions which cannot be performed efficiently if the operands are limited to the width and accessible number of general purpose registers. The present invention provides operands which are substantially larger than the data path width of the processor by using a general purpose register to specify a memory address from which at least more than one, but typically several data path widths of data can be read. The present invention also provides for the efficient usage of a multiplier array that is fully used for high precision arithmetic, but is only partly used for other, lower precision operations.

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